

Using interlaced restart reset cameras on Domino Iota, Alpha 2 and Delta boards

Documentation Addendum

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1. Introduction

1.1. CCD sensor technology

Active and storage array

A typical CCD is composed of two arrays:

- The active array: an array of photocells **permanently** integrating the charges resulting from the absorption of incoming light photons.
- The storage array: an array where charges are temporally stored and from which they are serially extracted during the readout phase.

CCD transfer – transfer gate

The **transfer gate** is a potential barrier that insulates the active array from the storage array. The transfer gate is opened once every field, during the frame blanking. Accumulated charges of selected active cells are transferred simultaneously to the corresponding cells of the storage array. This operation is named **CCD transfer**.

The CCD transfer **terminates the exposure** and **starts a new exposure** for the involved active cells. In other words, a CCD transfer clears the selected active cells and fills the storage array.

In case of progressive-scan sensors, **all** the active cells are transferred every CCD transfer. In case of interlaced-scan sensors, this is not always the case. See more explanations below.

CCD readout

This is the process where all the charges of the **storage array** are conveyed serially to the CCD output amplifier where they are converted into a voltage. This requires a complete field period to be completely achieved. At the end of the field period, the storage array is empty and ready for another CCD transfer.

CCD reset

Some CCD sensors are equipped with a CCD reset circuit.

When activated, it dumps the charges of **all** photocells of the active array to the substrate of the chip.

The CCD reset is not affecting the content of the storage array. However, it might disturb the output signals and therefore is usually performed during a line or frame blanking period

The CCD reset function is used to implement the electronic shutter facility. Charges of the active cells are dumped to the substrate a specified time before the CCD transfer. This time is the apparent exposure time.

1.2. Interlaced CCD sensors

This paragraph provides additional descriptions that are specific for interlaced CCD sensors.

Interlaced CCD readout - storage array

Interlaced cameras are characterized by the interlaced readout mechanism inherited from both European and US television standards.

The readout of a full resolution image, also called **frame**, is performed in two phases called “**fields**”: the **odd field** delivers the odd lines of the image; the even field delivers the even lines of the image.

The number of lines of cells of the storage array is **one-half** of the number of lines of cells in the active array.

Selective CCD transfer

The **Odd CCD transfer** initiates the readout of the odd-field; the Even CCD transfer initiates the readout of the even field.

In order to obtain a full-resolution image; it is required to perform both CCD transfers with the nominal interval of one-field period. Consequently, **not all pixels terminate the exposure simultaneously!**

Charge accumulation modes

Interline-transfer CCD sensors provide two modes of selection of the transferred active cells:

- The frame mode
- The field mode

According to the selected mode and the field parity, the transfer gate selects differently the active cells.

Frame mode

In frame mode, during the odd CCD transfer, only the charges from the odd lines of the active array are selected and transferred to the storage array. Similarly, during the Even CCD transfer, only the charges from the even lines are transferred to the storage array.

| Interlaced frame mode CCD transfers | | |
|-------------------------------------|------------------------------------|-------------------------------------|
| | <i>Frame mode Odd CCD transfer</i> | <i>Frame mode Even CCD transfer</i> |
| Storage array line #1 = | Active array line #1 | Active array line #2 |
| Storage array line #2 = | Active array line #3 | Active array line #4 |
| Storage array line #n = | Active array line #(2n-1) | Active array line #(2n) |

Consequently, in **frame** mode:

Pixels of the **even lines of the active array** accumulate charges during the interval between two **Even CCD transfers**.

Pixels of the **odd lines of the active array** accumulate charges during the interval between two **Odd CCD transfers**.

When camera is operated synchronously, the exposure time is 1 frame.

The exposure time of the 2 fields of image overlaps during the field period preceding the readout of the first field.

Field mode

In field mode, all the cells of the active array are selected for both CCD transfers. However a charge summation process of two adjacent active cells is performed during the CCD transfer.

For Odd CCD transfers, the n^{th} line of the storage array receives charges resulting from the summation of charges of the line# $2n$ with charges of the line# $2n-1$ of the active array.

For Even CCD transfers, the n^{th} line of the storage array receives charges resulting from the summation of charges of the line# $2n$ with charges of the line# $2n+1$ of the active array.

| Pseudo-interlaced field mode CCD transfers | | |
|--|--|--|
| | <i>Frame mode Odd CCD transfer</i> | <i>Frame mode Even CCD transfer</i> |
| Storage array line #1 = | Active array: line#1 + line#2 | Active array: line#2 + line#3 |
| Storage array line #2 = | Active array: line#3+ line#4 | Active array: line#4+ line#5 |
| Storage array line #n = | Active array: line#(2n-1) + line#(2n) | Active array: line#(2n) + line#(2n+1) |

Consequently, in **field** mode:

Pixels of the **active array** accumulate charges during the interval between two **CCD transfers** of any type

Pixels of the **odd lines of the active array** accumulate charges during the interval between two **Odd CCD transfers**.

When operated synchronously, the exposure time is 1 field.

The exposure time of the 2 fields of image never overlaps

Pseudo-interlacement effect is slightly reducing the vertical resolution.

Electronic shutter

Electronic shutter

For most the interlaced cameras equipped with an electronic shutter, the field mode is automatically invoked when the electronic shutter function is enabled.

Special electronic shutter

A few cameras, for instance the JAI CV-A50, allow specifying the frame integration mode when the asynchronous shutter is enabled.

This gives the capability to asynchronously reset the CCD and obtain a full-frame image from a single strobe flash.

2. Solution

2.1. Issues

Relative motion of the object

When the object moves relatively to the camera; a motion blur is likely to occur in the image. In order to minimize this nasty effect, following methods can be applied:

Reduce the camera exposure time.

Use strobe or intermittent lighting together with a low level ambient lighting.

Interlaced readout CCD sensor

All pixels of the full-resolution interlaced image have to originate from charges accumulated during a common exposure/illumination time.

Consequently, it is mandatory to select the **frame accumulation mode**.

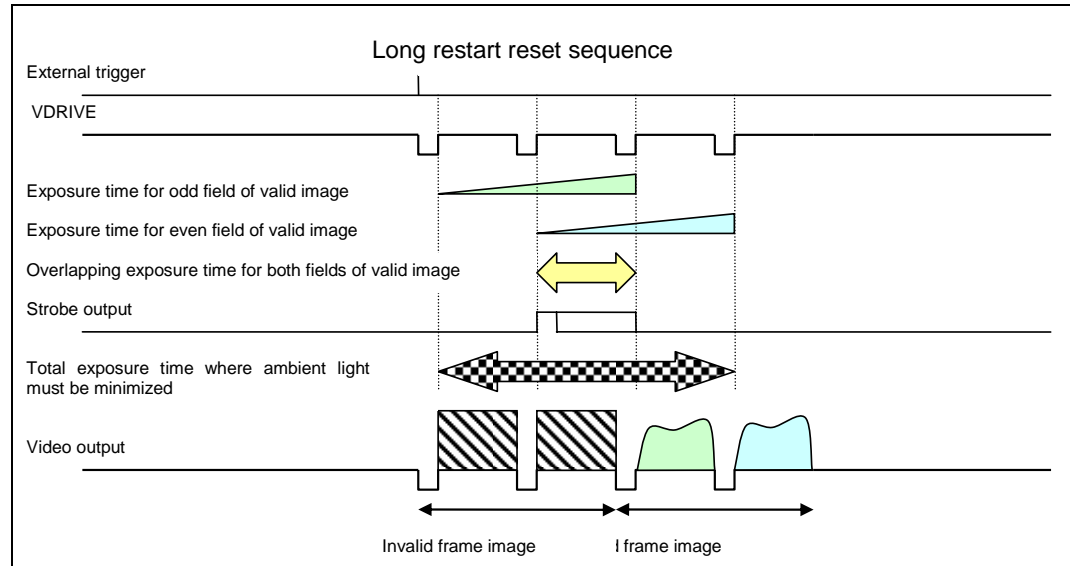
Asynchronous image capture

The camera has to deliver an image on occurrence of an externally supplied trigger signal.

On occurrence of trigger, a strobe flash has to be issued with the minimum possible delay and the resulting image must be readout as soon as possible. The best case is no delay; if not possible, it is better to have a fixed delay rather than a variable delay.

The interval between consecutive triggers has to be the smallest possible value in order to allow the maximum imaging rate.

2.2. Long Restart Reset sequence



The camera is configured for frame accumulation mode, the electronic shutter is disabled and the restart reset mode is enabled. The camera receives a permanent HDRIVE horizontal synchronization signal from the frame grabber.

On receipt of trigger, the frame grabber emits a series of **four** VD pulses at the nominal field rate of the camera.

The first VD pulse initiates a new exposure for the active cells of odd lines; this exposure will terminate at the third VD pulse.

During the interval between first and second VD pulse, the charges transferred in the storage array are moved serially towards the CCD output. The resulting video signal doesn't contain any useful information since it results from the exposure that occurs during the interval between two triggers. This field is discarded.

The second VD pulse initiates a new exposure for the active cells of even lines; this exposure will terminate at the fourth VD pulse.

During the interval between second and third VD pulse, the charges transferred in the storage array are moved serially towards the CCD output. The resulting video signal doesn't contain any useful information since it results from the exposure that occurs during the interval between two triggers. This field is also discarded.

Any light applied during the interval between second and third VD pulse will equally influence the video output during the third and fourth field. The strobe is issued at the beginning of this interval.

The third VD pulse initiated the readout of the first field of the acquired image. The fourth VD pulse initiates the readout of the second field of the acquired image.

Requirements

Camera must allow the Restart Reset mode; i.e. the capability to issue VD pulses asynchronously.

It is mandatory that the ambient light is sufficiently dimmed to avoid significant charge accumulation over a **2 fields period**.

The strobe flash or intermittent light equipment is controlled by the frame grabber strobe output.

Camera must be configured for frame accumulation mode.

Advantages

This method is applicable to a broad range of industrial camera since a majority allows the restart reset operation.

The ambient light and dark current noise influences the valid image during a moderate exposure time of 2 fields. Consequently, the requirements for the dark ambient are not so strong.

In addition, since the exposure time for both fields is the same, the ambient light and the dark current influences both fields in the same manner.

The delay between trigger and strobe is fixed.

Drawbacks

A low-level ambient lighting is required.

The delay between trigger and strobe is long; namely slightly more than a field period.

The maximum trigger rate is relatively slow; namely the field rate/4.

2.3. MultiCam

Since version 4.1.1, MultiCam implements the “Long restart reset sequence” for Domino Iota, Domino Alpha 2 and Domino Delta boards. This Domino operation mode is named “Restart Reset mode”.

Enabling Restart Reset mode

It is enabled when:

Expose=INTPRM

Readout=PLSTRG

It is applicable exclusively when

Scanning=INTERLACE

SyncMode=MASTER

GrabField=FRAME

The generic CAM file “InterlaceRR_lxxSM_R.cam” can serve as a template for a customized camera interface.

Using Restart Reset mode

The max trigger rate is 1/4 of the field rate of the camera. For instance a “50 Hz” camera will accept triggers up to 12.5 Hz.

A manual strobe output is available on the nominal strobe output pin; altering parameters TrueExp_us, StrobePos and SrobeDur parameters will allow the user to modify the position of strobe pulse. The illumination should occur exclusively into the second field.

The delivered CAM files are convenient for a 50 Hz camera.

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